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PTO/SB/33 (07-05)

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

550-299

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Stanley C. Spooner

Application Number

10/025,816

Filed

December 26, 2001

First Named Inventor

SLOBODNIK

Art Unit

2133

Examiner

J. Tabone, Jr.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

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The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ Applicant/Inventor
- ☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ Attorney or agent of record 27,393
(Reg. No.)
- ☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1.34 _____

Signature

Stanley C. Spooner

Typed or printed name

703-816-4028

Requester's telephone number

September 1, 2005

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

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**STATEMENT OF ARGUMENTS IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The following listing of clear errors in the Examiner's rejection and/or the Examiner's omissions of essential elements for a *prima facie* basis for rejection are responsive to the Final Rejection mailed June 2, 2005 (Paper No. 05232005) and are set out in correspondence with the errors as they exist chronologically in the Final Rejection.

**1. The Examiner has apparently failed to properly
construe the subject matter recited in Applicants'
independent claims 1 and 18.**

Applicants' independent apparatus claim 1 and method claim 18 requires "a self-test instructions specifying a test methodology." Claims 1 and 18 further require that the self-test controller be configurable "by said self-test instruction to implement different memory test methodologies." The Examiner appears to misunderstand the well-known definition of "methodology" as comprising a single step. The conventional definition of methodology is reflected in the definition contained in Webster's 9th New Collegiate Dictionary, i.e., "a body of methods, rules, and postulates employed by a discipline: a particular procedure or set of procedures. The emphasis in the definition is on the fact that methodology is not a single step, rule, or postulate and rather is a sequence of a plurality of steps, rules, and/or postulates, etc.

At no point in the final rejection does the Examiner construe the word "methodology" or the phrase "test methodology" to encompass only a single step, rule, or postulate. Moreover, the Examiner has also failed to support his interpretation of "methodology." Because claim terms are given their ordinary meaning, the Examiner is obligated to construe the term "methodology" as meaning a plurality of steps, tests, procedures, postulates, etc.

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In view of the above, the Examiner has improperly construed independent claims 1 and 18 suggesting that "test methodology" encompasses a single test or step or postulate.

2. The Lo reference clearly fails to include structures and method steps in the properly construed independent claims 1 and 18.

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

(a) Lo does not show or suggest a self-test controller which (is responsive to a self-test instructions specifying a test methodology) - The Examiner states in the final rejection page 4, section 4 that "Lo discloses that the ABIST engineer 12 (self-test controller) receives a 9 bit word 13 from a Micro-code Array 10 which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test instruction)." In effect, the Examiner alleges that one of the Lo 9 bit microcode words specifies the claimed "a test methodology."

However, in Lo, the Microcontroller stores up to eight 9-bit microcode words, but none of the 9-bit words can be used to specify a test "methodology" because they teach only a single step. In fact, all of the eight 9-bit Micro-code words are needed to implement a single test methodology.

The Lo reference provides various examples (1-17) as to how different test methodologies are implemented, e.g., a plurality (eight, in the listed examples) of the 9-bit words are needed in order to define each single test methodology. The Examiner has simply failed to point out where any test methodology is defined by the claimed single "self-test instruction" in the Lo reference. While the Examiner asserts that "a self-test instruction is used to specify a test

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methodology to be applied by the self-test controller" (final rejection page 3, lines 4 and 5), the Examiner does not indicate where this is present in the Lo reference. In fact, the Examiner fails to indicate anything in the Lo reference which comprises a "single self-test instruction" which specifies a test methodology which comprises a plurality of steps. At best, Lo contain a series of eight microcode words, each word specifying a single step and the accumulation of the eight microcode words specifies a test methodology.

As properly construed, the Examiner fails to point out how and where Lo teaches Applicants' claimed "self-test controller" which is "responsive to a self-test instruction specifying a test methodology."

(b) Lo does not teach a self-test controller which may be "configured by said self-test instruction to implement different memory test methodology." - As noted above, the Examiner misunderstands Lo teaching of a test methodology created by eight 9-bit microcode words with a single "self-test instruction" which specifies a test methodology comprised of a plurality of steps.

The Examiner does not indicate how or where there is any disclosure in the Lo reference of a self-test controller which "may be configured by said self-test instruction." Should Applicants have missed something in the Final Rejection which identifies a teaching in the Lo reference, an identification of the specific column and line number and, indeed, the number of the element alleged to be "self-test controller," the "self-test instruction" which specifies a "test methodology" is respectfully requested.

(c) There is no basis for rejection under 35 USC §102 - Absent a teaching of Applicants' claimed "self-test controller" in independent apparatus claim 1 or the "passing" step in independent method claim 18, the Examiner has failed to establish a prima-facie case of

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anticipation under 35 U.S.C. §102 and in any further rejection thereunder is respectfully traversed.

3. The Examiner does not allege that the missing teaching from Lo (of a "self-test controller" which is responsive to "a self-test instruction" which specifies a "test methodology") is taught in the Gold reference (US-2003/0167428 A1) or the Correale (US Patent 6,001,662).

If Applicants claimed subject matter (the element in claim 1 and the method step in claim 18) is missing from the Lo reference, it is incumbent upon the Examiner to demonstrate how or where that missing teaching is taught in the other cited references in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103.

Here, the Examiner has not indicated how or where either the Gold reference or the Correale reference teaches the missing subject matter from Applicants' specifically claimed "self-test controller." As a result, the Examiner does not have support for a *prima facie* case of obviousness under 35 U.S.C. §103.

4. The Examiner fails to provide any "reason" or "motivation" for combining any of the Lo/Gold/Correale references.

As set out in the case of *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998), the Court of Appeals for the Federal Circuit requires the Examiner "to show a motivation to combine the references that create the case of obviousness." The court goes on to note that "the Examiner must show reasons that the skilled artist, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

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The Examiner has simply ignored this requirement of showing some reasons or motivation for combining the bits and pieces of the Lo, Gold, or Correale references in the manner set forth in the final rejection. Thus, the Examiner has simply failed to set out a *prima facie* case of obviousness.

SUMMARY

Quite clearly, the Examiner has failed to properly construe the term "test methodology" set out in Applicants' claims 1 and 18, has ignored his obligation to show where the cited prior art references disclose the properly construed "self-test controller" and has failed to indicate how or why one of ordinary skill in the art would be motivated to combine two of the above three references. As a result, there is simply no support for any rejection of the independent claims 1 and 18 or the claims dependent thereon under 35 U.S.C. §102 or §103.

Applicants respectfully request that the Pre-Appeal Panel find that this application is allowed on the existing claims and prosecution remains closed.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

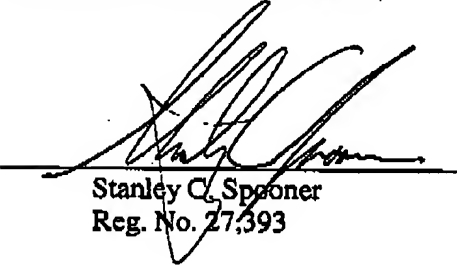
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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the Notice of Appeal, the Pre-Appeal Brief Request for Review Cover Sheet, and this five-page Statement are all being facsimile transmitted to the Patent and Trademark Office on the date shown below.


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